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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,419	08/29/2006	Shingo Maeda	062481	4383
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1250 CONNEC	TICUT AVÉNUE, NV	BROOKS, SHANNON		
SUITE 700 WASHINGTON, DC 20036		ART UNIT	PAPER NUMBER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary 10/598,419		Application No.	Applicant(s)					
Examiner SHANNON R. BROOKS 2617								
SHANNON R. BROOKS 2617 The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.	Office Action Summary	· ·						
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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (US 6573949 B1).

Consider Claim 1, Yamamoto teaches an isolation trap circuit (Col. 4-7) in which a PIN diode PD (Fig. 1, item 15) and an inductor L (Fig. 1, item 12) are connected in parallel to a first terminal 61 (Fig. 1, item 5a), and a capacitor C1 (Fig. 1, item 14) is connected in series to the inductor L (Fig. 1, item 12), while the PIN diode PD and the capacitor C1 are connected in parallel to a second terminal 62 (Fig. 1, item 5b), the isolation trap circuit being characterized in that a capacitor C2 (Fig. 1, item 13) is further connected and grounded between the first terminal 61 and the inductor L (grounded between the first terminal and the inductor through grounding resistor 16, Fig. 1, item 16 and Col. 6, lines 11-13), or between the inductor L and the capacitor C1, or between the capacitor C1 and the second terminal 62.

Consider **Claim 2**, Yamamoto teaches an isolation trap circuit (Abstract) in which a PIN diode PD (Fig. 1, item 15) and an inductor L (Fig. 1, item 12) are connected in parallel to a first terminal 61 (Fig. 1, item 5a), and a capacitor Cl (Fig. 1, item 14) is connected in series to the

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inductor L (Fig. 1, item 12), while the PIN diode PD and the capacitor C1 are connected in

parallel to a second terminal 62 (Fig. 1, item 5b), the isolation trap circuit being characterized in

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that a capacitor C2 is further connected and grounded between the inductor L and the capacitor

Cl (grounded between the first terminal and the inductor through grounding resistor 16, Fig. 1,

item 16 and Col. 6, lines 11-13).

Allowable Subject Matter

3. Claims 3-5 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

Conclusion

4. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to:**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window

Randolph Building

401 Dulany Street

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Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shannon Brooks whose telephone number is (571) 270-1115. The examiner can normally be reached on 7:30a.m. to 5p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nick Corsaro can be reached on (571) 272-7876. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

/Shannon R. Brooks/

Examiner, Art Unit 2617

Shannon Brooks

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June 1, 2009

/NICK CORSARO/

Supervisory Patent Examiner, Art Unit 2617